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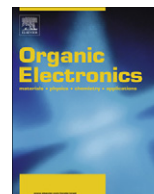

High permittivity dielectrics for poly(3-alkylthiophene) field-effect transistor devices

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ABSTRACT

In an attempt to disentangle the effects of permittivity and surface energy of the gate insulator (expressed by its dielectric constant k and water contact angle, respectively) on the performance of organic field-effect transistors (FETs), we fabricated top- and bottom-gate FET architectures with poly(3-alkylthiophenes) (P3ATs) of different side-chain lengths, using a range of gate dielectrics. We find that this class of semiconductor, including the short butyl-(C_4–) substituted derivative, is significantly less susceptible to the often detrimental effects that high-k dielectrics can have on the performance of many organic FETs. For bottom gate devices we identify the surface energy of the gate dielectric to predominantly dictate the device mobility.

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1. Introduction

In order to optimize organic field-effect transistors one should know the predominant factors that affect the charge transport in the active layer. This can be challenging as, typically, the charge-carrier mobility of the organic semiconductor is influenced in several intrinsic and extrinsic ways, which are normally interrelated. These can include surface roughness, the solid-state microstructure, molecular order, orientation and dipole disorder at the dielectric/semiconductor interface [1–12] For instance, surface roughness has been investigated for both small-molecule and polymeric organic semiconductors, including high-mobility pentacene [7] and poly(2,5-bis(3-alkylthiophen-2-yl)thieno-(3,2-b)thiophene) (PBTTT) [12] where it has been shown that a root mean square (RMS) roughness <0.5 nm is required for good transport. In addition, it has been demonstrated that an edge-on orientation and an increased degree of molecular order enhances the device performance of FETs based on, e.g., poly(3-hexylthiophene) (P3HT) [1] and pentacene [2].

A less clear relationship has been identified in literature where contrasting results have been published with respect to the influence of dielectric constant and polar disorder on device performance. In early work e.g., by Horowitz et al., a positive effect of dielectric permittivity on device mobility has been reported [13,14]. In contrast to this, Veres et al. found a negative effect of permittivity on transistor performance for devices based on amorphous poly(triarylamine)s (PTAA)s [3,5]. Subsequently a similar negative dependence on permittivity for P3HT [15], polycrystalline copper phthalocyanine thin films [9] to single crystals of rubrene [6,16] were reported. For the latter systems, different gate dielectrics were compared and it was

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found that low-k gate dielectrics result in the best FET performance despite having a reduced charge-carrier density. Establishing inter-correlations with other characteristics of the gate dielectric had, however, been a lesser focus of these studies.

Dipolar disorder in the dielectric seems often to be influential in or very close to the first layer of the semiconductor [16–18]. Valuably, Richards et al. [17] provided an analytical model that describes the effect of static dipolar disorder in polymer gate dielectrics on the density of states (DoS) of an adjacent organic semiconductor. The model gives an indication of the distance required for electronically decoupling the semiconductor from the insulating layer (approx. 0.5–1 nm). The experimentally found k-insensitivity of poly(5,5′-bis(3-dodecyl-2-thienyl)-2,2′-bithiophene) (PQT-12, with dodecyl-(C_{12}) substituents) [4], PBTTT with hexadecyl-(C_{16}) side chains [10] and poly{N,N′-bis(2-octyldodecyl)1,4,5,8-naphthalenedicarboximide-2,6-diyl}-alt-5,5′-(2,2′-bithiophene) P(NDI2OD-T2) with branched alkyl side chains ($C_{12}H_{25}$) [19] is in agreement with this model as the long alkyl substituents in these semiconductors can be expected to shield the material from the disordered states in the gate dielectric. For instance Chabinyc et al. [4] enabled the study of PQT-12 on hydrophilic SiO2 surfaces without the effects of processing on a disruptive high surface energy dielectric surface. This was done by de-laminating the semiconductor then transferring the top surface of the film to the bare SiO_2 surface. Identical mobilities were obtained for the de-laminated film compared to using an OTS self-assembled monolayer coated, hydrophobic surface. These results strongly suggest, as eluded to above, that despite the strong polar disorder formed by surface SiOH groups, PQT-12, possibly as a result of the long alkyl side chains, is unaffected by dipolar disorder.

In order to elucidate the capability of the side chains of polymer semiconductors to act as an intrinsic buffer layer to polar disorder from the gate dielectric [17] and to explore if we can differentiate the roles of energetic disorder in gate dielectrics from some of the other above-mentioned effects, especially surface energy, on device performance we fabricated FETs with P3ATs of different alkyl chain lengths. We selected the butyl-(C_4; P3BT), hexyl-(C_6; P3HT) and dodecyl-(C_{12}; P3DDT) derivatives, which, should provide a variation in the effective buffer layer thickness between ~0.5 nm (for P3BT) and 1.8 nm (P3DDT); *i.e.* a difference of up to 1.3 nm. (NB. The presence of any self-assembled monolayer deposited onto the dielectric should also be taken into account). In addition, to provide a fair comparison, we chose similar molecular weight polymers. We used differential scanning calorimetry (DSC) to demonstrate that each analog possessed a comparable propensity for crystallization (see Supplementary information).

To set a benchmark and to provide the first evaluation of the buffer layer thickness required for P3AT devices, two dielectrics of different k-value, *i.e.* thermally grown SiO_2 (k = 3.9) and plasma-enhanced chemical vapor deposited (PE-CVD) Si_3N_4 ($k \sim 6.5$) were selected for FET fabrication (see Table 1). Bottom-gate FET devices were first produced with the most investigated polymer in the P3AT series, *i.e.* regioregular P3HT, which was spin-coated from *ortho*-dichlorobenzene (*o*-DCB). This solvent was selected as it facilitates relatively long drying times and promotes microstructure ordering in the semiconductor [8]. Pre-patterned (lift-off) transistor structures with 10 μm channel lengths were thereby used as test architectures. The device fabrication and characterization were performed in N_2-atmosphere. Charge-carrier mobilities were calculated from the forward scan of a linear fit to the slope of $\sqrt{(I_{SD})}$ as a function of gate voltage (V_g) not exceeding −60 V, where I_{SD} is the drain current. [Note that the devices in this study were not optimized to reduce the affects of bias stress observed during the time-scale of device characterization].

In strong contrast to the previous work on organic FETs alluded to above, in which the device performance was reported to decrease where high-k gate insulators were utilized [3,5,6,9,15,16,20], we find that the high-k Si_3N_4-based devices displayed charge-carrier mobilities, μ_{FET}, that were approximately one order of magnitude higher than those measured for P3HT on the lower-k SiO_2 (Fig. 1a and Table 1). The question, therefore, arises of the origin of this discrepancy between the present results and literature. Clearly, the chemical nature and/or crystalline arrangement of the dielectrics used here could affect the device performance. For example, Li et al. [21] have demonstrated that the FET mobility in PQT-12 devices using a Si_3N_4 dielectrics can depend on the silicon content of the latter. This dependency was attributed to indirect effects of the silicon content on the Si_3N_4 insulator, such as surface roughness and quality of the OTS layer. It is important to note, though, that the difference in charge-carrier mobility found for the different Si_3N_4 devices was minor compared to the effect we observe in our P3HT transistors when varying the gate dielectric.

We, thus, set out to explore if the surface energy of the gate dielectric may play a critical role in P3AT devices since Si_3N_4 features a markedly different surface energy

Table 1
Summary of surface dielectric constants and water contact angles of the dielectrics used in the present study, and comparison of field-effect transistor mobilities realized with poly(3-butylthiophene) (P3BT), poly(3-hexylthiophene (P3HT) and poly(3-dodecyl thiophene) (P3DDT) using these insulators.

	μ_{FET} (P3BT) (cm^2/Vs)	μ_{FET} (P3HT) (cm^2/Vs)	μ_{FET} (P3DDT) (cm^2/Vs)	Dielectric constant k (–)	Water contact angle (°)
Bare SiO_2	3×10^{-5}	3×10^{-4}	3×10^{-3}	3.9 [5][a]	24
Bare Si_3N_4	2×10^{-4}	1×10^{-3}	8×10^{-3}	6.5[b]	36
HMDS SiO_2	3×10^{-3}	5×10^{-2}	1×10^{-1}	2.7–3.9[c]	82

[a] Ref. [5].
[b] Ref. [27].
[c] Ref. [22].

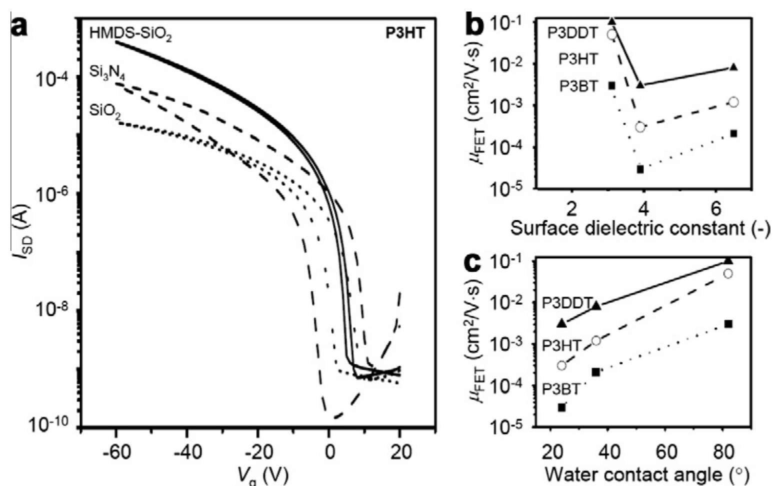

Fig. 1. (a) Transfer characteristics of poly(3-hexylthiophene) (P3HT) devices fabricated with three different gate insulators: Si_3N_4, SiO_2 and HMDS-treated SiO_2 (respectively, dotted, dashed and solid line), (b and c) Saturated mobility deduced for P3BT, P3HT and P3DDT bottom-gate bottom-contact devices plotted against (b) the dielectric constant of the three insulators used to fabricate such bottom-gate FETs and (c) their water contact angle.

compared to SiO_2. The latter manifests itself by different water contact angles observed for the two materials (36 and 24 for Si_3N_4 and SiO_2 respectively; see Table 1). In addition to bare SiO_2 and Si_3N_4 FETs, we also fabricated devices comprising a SiO_2 gate dielectric that were surface-treated with hexamethyldisilazane (HMDS) before application of the P3HT. This allowed us to alter the surface energy of SiO_2 (water contact angle = 82; Table 1). Note, though, that according to Ting et al. [22] the dielectric constant may have slightly been altered by the HMDS treatment, resulting in a marginally lower *k*-value compared to bare SiO_2.

It is evident from the device characteristics displayed in (Fig. 1a), that the charge-carrier mobility measured for HMDS-treated SiO_2 devices is higher compared to both Si_3N_4 and bare SiO_2-based FETs by approximately one and two orders of magnitude respectively; (see Fig. 1b and Table 1). No apparent dependency of μ_{FET} with the *k*-value of the dielectric was found. We therefore plotted μ_{FET} *vs.* the water contact angle of the respective gate insulator. A monotonical trend was found in accordance with previous literature [5,23,24], showing μ_{FET} increasing with hydrophobicity of the dielectric (Fig. 1c). This indicates that the surface energy has indeed a stronger influence on *P3HT* device performance than the polar disorder at the surface of the gate dielectric.

We further scrutinized our observation of μ_{FET} apparently increasing with decreasing surface energy of the gate dielectric by preparing devices with other P3ATs – *i.e.* P3BT and P3DDT (Fig. 2a). Reassuringly, the dependence of charge carrier mobility on the aforementioned dielectrics was found to be essentially identical to the one observed for P3HT; *i.e.* we find again μ_{FET} (HDMS-treated SiO_2) > $\mu_{FET}(Si_3N_4)$ > μ_{FET}, (SiO_2) (Fig. 2a inset and Table 1). P3DDT was thereby consistently found to display the best device performance. Note though, that the high mobility for this analog is not attributed to shielding from interfacial polar disorder despite the relatively long insulating dodecyl side chains in P3DDT. If shielding was one of the factors dominating charge transport, the P3AT FETs based on the high-*k* Si_3N_4 dielectric should display the lowest mobility. This should be especially true for the short-chain substituted P3BT [3,5]. However, for all P3ATs, including P3BT, we observe the lowest devices performance for the bare SiO_2 devices. [NB. For low-*k* dielectrics, the polar disorder coupling length is calculated to be below 0.5–1.0 nm

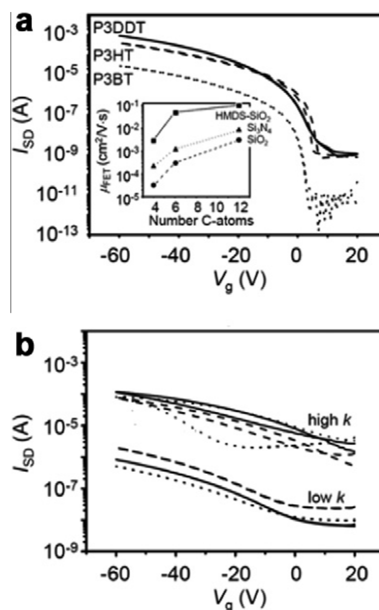

Fig. 2. (a) Transfer characteristics of P3BT, P3HT and P3DDT bottom-gate transistors fabricated with HMDS-treated SiO_2. The inset shows the dependence of charge-carrier mobility on length of the alkyl side chains. (b) Top-gate device data using a high-*k* and a low-*k* organic dielectric (P3BT dotted, P3HT: dashed, and P3DDT solid line). (Note that a lower off-current may be expected for the high-*k* dielectric device as the larger electric field should result in a greater ability to deplete charge carriers in the bulk. However we observe a higher off-current, which is most likely due to doping effects caused by the highly polar nature of this dielectric, which was fabricated in ambient conditions [25,26].)

[17], which is comparable to the buffer layer thickness provided by butyl side chains. This buffer layer would be expected, however, to be insufficient to shield from polar disorder of high-*k* dielectrics such as Si_3N_4. Furthermore the three polymer analogs behave indifferently when considering the dependence of mobility on permittivity.]

Since the model proposed by Richards et al. [17] was specifically developed for amorphous polymer dielectrics and should not strictly be applied to the inorganic dielectrics used in the above described devices, especially those based on crystalline Si_3N_4 dielectrics, we fabricated top-gate FETs in a second series of experiments. Two solution-processable organic materials were this time selected for the gate dielectric, which unlike the inorganic dielectrics utilized above are suitable for roll-to-roll processing; *i.e.* a significantly high-*k*, acetone-soluble cyanoresin ($k \sim 18$) and the low-*k*, commercially available, fluoropolymer Cytop™ ($k = 2$) were used for device fabrication. Top-gate/top-contact FET devices of 50 µm channel lengths were prepared from *o*-DCB solutions of P3BT, P3HT and P3DDT, which were produced in an air atmosphere with short processing times to minimize doping. For the two dielectrics the permanent dipole was assumed to be approximately twice as large for the cyanoresin as it is for Cytop™ (see Supplementary information). Therefore, a significant dipolar disorder could be expected for devices comprising the cyanoresin dielectric. This would result in a pronounced broadening of the (DoS) distribution (Supplementary information) and, thus, lower device mobilities. However, experimentally no significant dependence of device performance with the length of side chain substituent was found for the high-*k* devices (or for the low-*k* architectures). Indeed, for a given dielectric all three P3ATs featured very similar FET characteristics with essentially identical threshold voltages, sub-threshold slopes and ON/OFF ratios. A significantly higher source–drain current I_{DS} (10^{-4} *vs.* 10^{-6} A) is observed for the high-*k* compared to the low-*k* dielectric transistors, indicating a higher μ_{FET} for the former architecture (Fig. 2b) The mobility values for our top-gate devices are summarized in Table 2).

Clearly our top-gate device data is in line with our results on P3AT bottom-gate devices. However, again, our data is in contrast to previous work on other organic FETs [3,5,6,9,15,16,20]. Our results therefore suggest that provided the surface energy of the gate dielectric is kept low, for certain organic FETs high-*k* dielectrics can be utilized, even when semiconductors are selected, which do not necessarily contain long alkyl side chains. This is important indicating that high μ_{FET} is not exclusive to low permittivity dielectrics or semiconductors with relatively long alkyl side chains.

Table 2
Comparison of field effect transistor mobility obtained using a high and low-*k* dielectric for three PAT analogs in a top-gate device geometry. Forward scans from transfer characteristics in the saturated regime were used to calculate mobility.

	μ_{FET} (P3BT) (cm^2/Vs)	μ_{FET} (P3HT) (cm^2/Vs)	μ_{FET} (P3DDT) (cm^2/Vs)
$k = 2$ (cytop)	0.014	0.05	0.03
$k = 18$ (cyanoresin)	0.07	0.07	0.07

In summary, by varying the hetero-interface distance in polymer FETs using a series of P3ATs in combination with high- and low-*k* dielectrics in top and bottom gate configurations, we found that the C_{12}-substituted P3DDT consistently displayed higher mobilities than P3HT and P3BT. Longer substituents, such as in P3DDT, may be expected to provide sufficient shielding from polar disorder found in high-*k* dielectrics, however, no obvious dependency of μ_{FET} with *k*-value of the gate dielectric was found even for the short-chain substituted P3BT. In bottom-gate devices, the charge-carrier mobility monotonically increased with the insulators' surface contact angle and, again, an identical trend was found for all three P3ATs. This strongly indicates that the surface energy had the overriding affect on the device performance. The model for DoS broadening [17] may thus not be applicable to the P3ATs class of semiconductors. The hexyldecyl-P3AT derivative (P3HDT) is now being synthesized to further investigate the origin of the apparent anomalous behavior of P3ATs compared to other organic semiconductors. Our finding, therefore, may be exploited in future with respect to selection of suitable surface treatments for existing gate dielectrics or design of new, high-performance flexible dielectrics suited to roll-to-roll processing for low-cost printed electronics.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.orgel.2011.11.001.

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